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Claims

[c1] A method of forming a substantially planar multiple crystallographic orientation SOI substrate comprising:
providing a multiple orientation surface atop a single orientation layer, said multiple orientation surface comprising a first device region contacting and having a same crystal orientation as said single orientation layer, and a second device region separated from said first device region and said single orientation layer by an insulating material, wherein the first device region and the second device region have different crystal orientations;
forming a damaged interface in said single orientation layer;
bonding a wafer to said multiple orientation surface;
separating said single orientation layer at said damaged interface, wherein a damaged surface of said single orientation layer remains; and
planarizing said damaged surface until a surface of said first device region is substantially coplanar to a surface of said second device region.

[c2] The method of Claim 1 wherein said providing said multiple orientation surface atop said single orientation layer

comprises:

providing a bonded substrate comprising at least a semiconductor layer having a first crystallographic orientation and said single orientation layer of a second crystallographic orientation separated by an insulating layer, said first crystallographic orientation is different from said second crystallographic orientation;

protecting a portion of the bonded substrate to define said second device region, while leaving another portion of the bonded substrate unprotected;

etching said unprotected portion of the bonded substrate to expose a surface of said single orientation layer;

forming said insulating material around said second device region;

regrowing a semiconductor material on said exposed surface of the single orientation layer to produce said first device region having the same crystal orientation as the single orientation layer; and

planarizing the bonded substrate so that the first device region is substantially planar with an the second device layer.

[c3] The method of Claim 2 wherein said semiconductor material is formed utilizing a selective epitaxial growth method.

[c4] The method of Claim 1 wherein said forming said damaged interface in said single crystal orientation layer comprises implanting hydrogen ions.

[c5] The method of Claim 1 wherein said bonding said wafer to said multiple orientation surface comprises:
depositing an oxide layer atop said multiple orientation surface;
planarizing said oxide layer;
contacting said wafer to said oxide layer; and
heating said wafer contacting said oxide layer under conditions that are capable of bonding.

[c6] The method of Claim 5 wherein said conditions that are capable of bonding comprise heating at a temperature from about 200°to about 1050°C for a time period from about 2 hours to about 20 hours in an inert atmosphere comprising He, Ar, N_2, Xe, Kr or a mixture thereof.

[c7] The method of Claim 2 further comprising a planarization stop layer separating said semiconducting layer and said insulating layer, wherein said planarization stop layer is etched during defining of said second device region so that said planarization stop layer is positioned between said second device region and said insulating layer.

[c8] The method of Claim 7 wherein said planarizing comprises:
chemical mechanical polishing said damaged surface stopping on said planarization stop layer;
forming a thermal oxide layer on said first device region, wherein said thermal oxide layer is coplanar with said planarization stop layer; and
removing said planarization stop layer and said thermal oxide layer by etching.

[c9] The method of Claim 1 wherein said first device region is in a (110) crystal plane and said second device region is in a (100) crystal plane.

[c10] The method of Claim 1 wherein said first device region is in a (110) crystal plane and said second device region is in a (100) crystal plane.

[c11] The method of Claim 1 wherein said first device region is in a (100) crystal plane and said second device region is in a (110) crystal plane.

[c12] The method of Claim 11 wherein said first device region comprises on nFET and said second device region comprises a pFET.

[c13] A semiconducting structure comprising:

a substantially planar SOI substrate comprising a first device region having a first crystallographic orientation and a second device region having a second crystallographic orientation, said first crystallographic orientation being different from said second crystallographic orientation; and

an isolation region separating said first device region from said second device region.

[c14] The semiconducting structure of Claim 13 wherein said first device region has a first device thickness and said second device region has a second device thickness, wherein said first device thickness is equal to said second device thickness or said first device thickness is different from said second device thickness.

[c15] he semiconducting structure of Claim 13 wherein said first crystallographic orientation is in a (110) crystal plane and said second crystallographic orientation is in a (100) crystal plane.

[c16] The semiconducting structure of Claim 15 wherein said first device region comprises a pFET and said second device region comprises an nFET.

[c17] 17. The semiconducting structure of Claim 13 wherein said first crystallographic orientation is in a (100) crystal

plane and said second crystallographic orientation is in a (110) crystal plane.

[c18] The semiconducting structure of claim 17 wherein said first device region comprises an nFET and said second device region comprises a pFET.

[c19] An integrated circuit comprising:
a substantially planar SOI substrate comprising a first device region having at least one nFET device on an nFET optimized surface and a second device region having at least one pFET device on a pFET optimized surface, wherein said nFET optimized surface has a crystallographic orientation different from said pFET optimized surface; and
an isolation region separating said first device region from said second device region.

[c20] The integrated circuit of claim 19 wherein said nFET optimized surface has a (100) crystal plane and said pFET optimized surface has a (110) crystal plane.